ABSTRACT

ONE-DIRECTIONAL NORMALLY-ON VERTICAL SILICON CARBIDE MESFET

ON SILICON SUBSTRATE

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The main objective of this thesis is to design a one-directional normally-on vertical 3C-SiC MESFET on silicon substrate. The 3C-SiC material has higher carrier mobility, high saturation velocity and high critical breakdown field compared to traditional silicon devices. Epitaxial layer of 3C-SiC can be easily grown on the large area of silicon wafer. Vertical MESFET occupies less than 33% of the area compared to lateral MESFET with same dimensions, and this increases the integration density and reduces the cost. The drain current of vertical 3C-SiC MESFET is 100% higher than lateral structure MESFET with same dimensions. Vertical 3C-SiC MESFETs can be easily connected in parallel in order to get higher currents and can be easily cooled, since the junctions are exposed.

This work involves the study of electrical and thermal characteristics of the device. Electrical characteristics of the device are investigated using Silvaco Atlas software. Thermal nature of the device is studied using COMSOL Multiphysics. Numerical calculations were done in MATHCAD. The device breakdown voltage was simulated at gate voltage of 0V and found to be more than 600V. The drain current reached 600mA/mm, with a critical breakdown electric field of 3.9x10^6 V/cm.
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ONE-DIRECTIONAL NORMALLY-ON VERTICAL SILICON CARBIDE
(3C-SiC) MESFET ON SILICON (Si) SUBSTRATE

BY
RAMANA THAKKALLAPALLY

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Thesis Director:
Ibrahim Abdel-Motaleb
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I would like to thank my parents, brother, sister, and cousin for the love and care they have been showing over the course of my life. Finally, I thank Almighty for giving me the strength and good health to pursue this endeavor.
DEDICATION

To my parents
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CHAPTER 1
INTRODUCTION

1.1. Introduction to power semiconductor devices

The increasing reliance of the modern world on electronic appliances for health care, comfort and transportation has brought great advances in generation of power, distribution of power and managing power technologies. After the replacement of vacuum tubes by solid state devices in 1950, the power semiconductor industry depends upon silicon bipolar devices such as bipolar power transistors and thyristors [1]. Due to advancement in technology, their power ratings are increased, and their fundamental limitations in terms of control and protection circuits lead to an increase in cost and decrease of the efficiency of the system.

In 1970, silicon MOS technology played a vital role in the semiconductor industry. MOSFET used for high-frequency and low-voltage (<100) applications [1]. After that, MOS and bipolar technology combined and a new device came to the market, i.e., IGBT (insulated gate bipolar transistor). It is used for medium-power applications [2]. The high power density and ruggedness of IGBT used for high-voltage DC transmission systems. From Figure 1.1, as a system operating frequency increases, the system power rating starts decreasing. From Figure 1.1, HVDC power transmission has high power rating ($10^8$ Volt-Amps), and it operates at low frequencies ($10^2$ Hz). Microwave power devices operate at higher frequency with low power rating. The hybrid electric vehicles have a lot of applications, and they operate at medium-power applications.
Silicon power devices have served the power semiconductor industry for over five decades, but they cannot be considered to have ideal device characteristics. As ideal power rectifier in forward conduction mode, it should carry some current with zero voltages. In reverse blocking mode, it should have some amount of voltage with zero current, and finally, the ideal power rectifier should switch between on-state to off-state with zero switching time [1]. In silicon power rectifier, there is some voltage drop in conduction mode and leakage current in reverse blocking mode; this leads to conduction losses in the silicon power rectifier. In addition to that, the thickness of the drift region and doping concentration should be carefully chosen in order to achieve target breakdown voltage. In silicon power devices, power dispassion increases when the voltage rating increases, which leads to increase in voltage drop.
In bipolar power devices, during the on-state condition, there is an injection of minority carriers. These carriers must be removed when the device status changes from on-state to off-state and this is done by charge removal through a gate drive current or an electron hole recombination process. This entire process leads to the introduction of a significant power loss that degrades power management efficiency [1]. It is, therefore, preferable to utilize the unipolar power devices in the power semiconductor industry. The commonly used unipolar device is the Schottky rectifier that uses the metal semiconductor barrier to produce the current rectification. Silicon Schottky rectifiers are available with blocking voltage of 100 volts; beyond this value on-state voltage drop increases and it leads to degraded system efficiency.

Silicon carbide (SiC) Schottky rectifiers have lower drift region resistance, and they can design high-voltage power devices with low on-state voltage drop. Silicon power MOSFET has low on-state resistance. The drift region resistance increases with an increase in system blocking voltage and this limits the performance of silicon power MOSFET to below 200 volts. Several groups of scientists worked on the development of bipolar junction transistors (BJT) [3-6] and GTOs [7-8] using silicon carbide (SiC). Due to the large junction potential for silicon carbide, it leads to an increase in on-state voltage drop compared to commercially available silicon devices.

The most widely used silicon high-voltage (>300 volts) power semiconductor device is IGBT (insulated gate bipolar transistor). The development of IGBT in silicon carbide (SiC) has been analyzed by several groups of scientists. The large junction potential and high resistance of P+ region in silicon carbide results in high on-state voltage drop compared to silicon devices and also compromised switching speed compared to silicon devices. The unipolar devices
contain drift regions that are designed to support the blocking voltage. The resistance of the ideal drift region can be related to the basic properties of semiconductor material.

Figure 1.2. Specific on resistance of ideal drift region [1].

The maximum voltage that can be supported by the drift region is determined by the maximum electric field ($E_M$) reaching the critical breakdown electric field and doping concentration, this determining the maximum depletion width ($W_D$) [1].

$$R_{on-ideal} = \frac{4.BV^2}{\varepsilon_s\mu_n E_c^3}$$ (1.1)

where $BV$ is the breakdown voltage of the device, and the denominator of the equation $\varepsilon_s\mu_n E_c^3$ is called Baliga’s Figure of merit for power devices (BFOM) [1]. It indicates the impact of semiconductor material properties on resistance of the drift region. The drift region resistance dependence is inversely proportional to the mobility of power semiconductor material (generally electron mobility has greater than hole mobility) such as gallium arsenide (GaAs)
and SiC. Stronger (cubic) dependence is the resistance of the critical electric field for breakdown, which favors wide band gap semiconductors such as silicon carbide (SiC).

From the Figure 1.2 specific on-state resistance of various semiconductors such as silicon, gallium arsenide and silicon carbide are compared. The drift region resistance of GaAs in comparison to silicon is due to greater mobility for electrons. The advancement of drift region resistance for SiC in comparison with silicon is due to large critical electric fields for breakdown. Based on the above considerations, silicon carbide plays a vital role in the modern semiconductor power industry.

1.2 Introduction to silicon carbide material properties and technology

Silicon carbide (SiC) devices have received increased attention for high-power, high-speed, high-voltage and high-temperature applications due to their excellent properties, including wide band gap, high electron saturation velocity, and high thermal conductivity [9-10]. 3C-SiC power devices have high breakdown electric field strength compared to silicon-based power devices. The high breakdown field allows SiC devices to operate at much higher voltages than Si or GaAs power devices and to have significant RF output power at high temperatures [11].

In the area of power semiconductors, Si devices can usually provide either high speed (Schottky barrier diodes) or high breakdown (p-i-n diodes), but not both. In principle, SiC can provide both of these characteristics. We have been investigating the feasibility of combining SiC films with Si substrates for the eventual integration of SiC high-power, high-temperature devices with Si integrated circuit signal processing. This approach also produces a large SiC area for the device fabrication without the need for the development of large-diameter crystals.
The epitaxial growth of SiC on a silicon substrate is a study object of great interest due to the possibility it offers to electrical and electronic engineering applications. SiC exists in over 200 polytypes. Of these, the three most widely investigated polytypes are 3C-SiC, 4H-SiC and 6H-SiC. 3C-SiC is a good object for research and development in high-voltage, and high-temperature applications because it has lot of unique properties. Table 1.1 shows these properties in comparison with commonly used semiconductor materials [12].

Table 1.1: PHYSICAL PROPERTIES OF VARIOUS SEMICONDUCTORS POWER DEVICES [12]

<table>
<thead>
<tr>
<th>Material</th>
<th>$E_g$ (eV)</th>
<th>$\mu_n$ (cm²/V.s)</th>
<th>$\mu_p$ (cm²/V.s)</th>
<th>$v_{sat}$ (cm/s)</th>
<th>$E$ (V/cm)</th>
<th>$\lambda$ (W/cm.k)</th>
<th>$\varepsilon_r$</th>
</tr>
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<tr>
<td>Si</td>
<td>1.12(i)</td>
<td>1450</td>
<td>450</td>
<td>$10^2$</td>
<td>3x10⁵</td>
<td>1.3</td>
<td>11.7</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.4(d)</td>
<td>8500</td>
<td>400</td>
<td>$2x10^2$</td>
<td>4x10⁵</td>
<td>0.54</td>
<td>12.9</td>
</tr>
<tr>
<td>3C-SiC</td>
<td>2.3(i)</td>
<td>1000</td>
<td>45</td>
<td>$2.8x10^7$</td>
<td>4x10⁶</td>
<td>5</td>
<td>9.7</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>2.9(i)</td>
<td>415</td>
<td>90</td>
<td>$2x10^7$</td>
<td>2.5x10⁶</td>
<td>5</td>
<td>9.7</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>3.2(i)</td>
<td>950</td>
<td>115</td>
<td>$2x10^7$</td>
<td>3x10⁶</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>GaN</td>
<td>3.39(d)</td>
<td>1000</td>
<td>350</td>
<td>$2x10^7$</td>
<td>5 x 10⁶</td>
<td>1.3</td>
<td>8.9</td>
</tr>
<tr>
<td>GaP</td>
<td>2.26(i)</td>
<td>250</td>
<td>150</td>
<td>$1.25x10^7$</td>
<td>1x10⁷</td>
<td>1.1</td>
<td>11.1</td>
</tr>
<tr>
<td>C</td>
<td>5.6(i)</td>
<td>2200</td>
<td>1800</td>
<td>$3x10^7$</td>
<td>5.6x10⁷</td>
<td>20</td>
<td>5.7</td>
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From Table 1.1, the properties of 3C-SiC are superior compared to silicon, GaAs, and GaP semiconductor materials.
The energy band-gap of 3C-SiC is double that of silicon. The energy band-gap plays an important role in calculating the breakdown voltage; 3C-SiC has high breakdown voltage due to wide energy band-gap [14]. The saturation velocity of 3C-SiC is high compared to all other semiconductor material. Saturation velocity of electrons controls the drain current in short-channel devices. Critical breakdown electric field of 3C-SiC is double that of silicon semiconductor material [15]; it also plays an important role in calculating the breakdown voltage. 3C-SiC material has higher heat conducting capacity than copper at room temperature. SiC can be easily oxidized to grow high-quality SiO$_2$ layers.

Reduction of power dissipation in the conversation systems is strongly required for energy saving. In particular, high-voltage power converters with high efficiency are essential to realizing a stable and highly efficient electric power network by optimizing the use of solar power and wind-generated power in the future.

Figure 1.3 Comparison of individual semiconductor features [13].
Silicon carbide (SiC) is a newly emerging wide band gap semiconductor by which high-voltage power devices can be realized owing to its excellent properties. The major features of SiC power devices include low on-resistance, fast switching speed, high-voltage blocking capability and high-temperature operation. The on-resistance of SiC material is 100 times lower than Si material. The breakdown voltage of SiC-based power devices is eight times higher than Si-based power devices. For ultrahigh-voltage applications above 6000 V, SiC bipolar devices will be attractive. Through recent progress in crystal growth and device technologies, 600-1700V class SiC power switching devices as well as diodes are now commercialized by several manufacturers.

Figure 1.4. Major territories of individual unipolar and bipolar power devices for Si and SiC in terms of the rated blocking voltage [14].
1.2.1 Energy band gap

Energy band gap of silicon carbide (SiC) is larger than that of silicon, and it is considered to be wide band gap semiconductor. The band gap of 3C-SiC is 2.3 V, which is double that of silicon, since large band gap results in smaller generation of carriers in the depletion region of devices and is favorable for reducing the leakage current of devices. The large band gap results are beneficial for producing metal-semiconductor contacts with Schottky barrier heights; this enables reduction of leakage current in MESFET and the Schottky rectifier.

1.2.2 Intrinsic carrier concentration

The intrinsic carrier concentration is determined by the thermal generation of electron hole pairs across the energy band gap of semiconductor material [1]. $N_C, N_V$ are density of states...
in conduction and valance band respectively. $E_G$ is the energy band gap; $K$ is the Boltzmann’s constant and $T$ is the absolute temperature.

For silicon \[ n_i = 3.87 \times 10^{16} T^{3/2} e^{-(7020)/T} \] \hspace{1cm} (1.2)

For 4H-SiC \[ n_i = 1.70 \times 10^{16} T^{3/2} e^{-(2080)/T} \] \hspace{1cm} (1.3)

Using these equations, intrinsic concentration is calculated as a function of temperature. It is clear that the intrinsic concentration for silicon carbide is smaller than that of silicon due to the large difference in band gap energy at 300K. The intrinsic concentration for 4H-SiC is $6.7 \times 10^{-11}$, while that for silicon is $1.4 \times 10^{-10}$ [1]. This gives bulk generation current negligible for determination of leakage current in silicon carbide semiconductor devices. The built-in potential of silicon carbide is larger than that of silicon due to the smaller values of intrinsic carrier concentration.

1.2.3 Impact ionization constants

The main advantage of wide band gap semiconductors for power device applications is the greater breakdown voltage capability of the material. The high breakdown voltage is associated with the reduced ionization coefficients at any electric field compared to silicon. The impact of ionization rate for electrons is larger than holes in silicon semiconductor material, but for silicon carbide the opposite is true.

Impact of ionization coefficients are calculated using Chynoweth’s law:

\[ \alpha = a.e^{-b/E} \] \hspace{1cm} (1.4)

where $E$ is the electric field in the direction of current flow and the parameters $a$, $b$ are constants that depend upon temperature and semiconductor material. For silicon, the impact of ionization
is measured as a function of temperature and electric field. The measured impacts of ionization coefficients of silicon at room temperature are $a = 7 \times 10^5 \text{V/cm}$, $b = 1.23 \times 10^6 \text{V/cm}$ [1]. The impact of ionization coefficients for silicon carbide is measured as a function of temperature and electric field using electron beam excitation method [1]. Impact of ionization coefficients of holes in 4H-SiC is given by [1]

\[
a (4H\text{-SiC}) = 6.46 \times 10^6 - 1.07 \times 10^4 \\
b (4H\text{-SiC}) = 1.75 \times 10^7
\] (1.5)

The impact of ionization occurs at lower electric fields in silicon compared to 4H-SiC. As a result, the breakdown of the 4H-SiC device occurs at 2-3 MV/cm, which is more than that of silicon. From the Table 1.1 the breakdown electric field of 3C-SiC is $4 \times 10^6 \text{ V/cm}$. The high breakdown field of 3C-SiC gives more breakdown voltage. The breakdown voltage is determined by making ionization integral to unity [1]:

\[
\int_0^w a \cdot dx = 1
\] (1.7)

where $a$ is the impact of the ionization coefficient. To obtain the exact solution for breakdown voltage, it is convenient to replace Chynoweth’s law to Fulop’s power law relation for silicon semiconductor [1].

\[
\alpha_F (\text{Si}) = 1.8 \times 10^{-35} E^7
\] (1.8)

For 4H-SiC, Baliga’s power law relation for impact of ionization coefficient is (Figure 1.6):

\[
\alpha_B (4H\text{-SiC}) = 3.9 \times 10^{-42} E^7
\] (1.9)
Figure 1.6. Impact of ionization of silicon and 4H-SiC using power law [1].

From the power law equation breakdown voltage, maximum depletion layer width is derived [1]:

\[
BV_{pp}(4\text{H-SiC}) = 3.0 \times 10^{15} \times N_D^{-3/4} \tag{1.10}
\]

\[
W_{pp}(4\text{H-SiC}) = 1.82 \times 10^{11} \times N_D^{-7/8} \tag{1.11}
\]

where \(BV_{pp}\), \(W_{pp}\) is the breakdown voltage and maximum depletion layer width respectively. The ratio of breakdown voltage of 4H-silicon carbide to silicon for same doping concentration is given as 56.2. It is possible to use much higher doping concentration in 4H-SiC compared to silicon. The ratio of doping concentration of 4H-SiC to silicon for the same breakdown voltage is given as 200.

For same doping concentration, the maximum depletion width in 4H-SiC is 6.8 times larger than that of silicon because it can withstand much higher electric field. The smaller
depletion width with larger doping concentration results in an enormous reduction in specific on-state resistance in 4H-SiC compared to silicon.

1.2.4 Critical Electric Field

The critical electric field is related to the impact of ionization rate, which increases as the carrier energy exceeds the band-gap [2]. Due to the large band-gap the critical breakdown electric field SiC is 10 times larger than that of silicon and GaAs. The critical breakdown electric field of the 4H-SiC is given by (Figure 1.7) [1]:

$$E_{C} (4H-SiC) = 3.3 \times 10^4 N_D^{1/8}$$  \hspace{1cm} (1.12)

Figure 1.7. Critical electric field for breakdown versus doping concentration [1].
1.2.5 Electron Mobility

The mobility of electrons is larger than holes in 3C-SiC semiconductor material (Figure 1.8); therefore, it is favorable to make the unipolar device with N-type drift region rather than P-type drift region.

The specific resistivity of drift region is given by the relation [1]:

$$\rho_n = \frac{1}{q \mu_n N_d}$$  \hspace{1cm} (1.14)

Where \(\mu_n\) is the mobility of electrons, \(N_D\) is the doping concentration, \(q\) is the charge of electrons, and \(\rho_n\) is the specific resistivity of the 3C-SiC material.

$$\rho_n = \frac{1}{\sigma_n}$$  \hspace{1cm} (1.15)

Where \(\sigma_n\) is conductivity of the 3C-SiC material.

Figure 1.8. Mobility of electrons in 4H-SiC and silicon [1].
From the Figure 1.9, mobility decreases with an increase in temperature due to enhanced columbiaic scattering of electrons by ionized donors. For silicon, the mobility of electrons as a function of doping concentration is given by relation [1]:

\[
\mu_n(Si) = \frac{(5.10 \times 10^{18} + 92 N_D^{0.91})}{(3.75 \times 10^{15} + N_D^{0.61})}
\] (1.15)

For silicon carbide (3C-SiC), the mobility of electrons as a function of doping concentration is given as [1]:

\[
\mu_n(4H-SiC) = \frac{(4.05 \times 10^{13} + 20 N_D^{0.61})}{(3.55 \times 10^{10} + N_D^{0.61})}
\] (1.16)

From the Figure 1.9, due to the enhanced phonon scattering, mobility of semiconductor decreases with increase in temperature.

Figure 1.9. Mobility of 4H-SiC, silicon versus Temperature [1].

For silicon, temperature dependence of mobility at low doping concentration is given by [1]:

\[
\mu_n(Si) = 1360 \left(\frac{T}{300}\right)^{-2.42}
\] (1.17)
For 4H-SiC, temperature dependence of mobility at low doping concentration is given by [1]:

\[ \mu_n(4H\text{-SiC}) = 1140\left(\frac{T}{300}\right)^{-2.70} \]  \hspace{1cm} (1.18)

1.2.6 Thermal conductivity

The thermal conductivity is an important parameter in power semiconductor devices. It is used to transport the heat in the device. The semiconductor materials such as GaN have low thermal conductivity compared to silicon. The thermal conductivity of SiC is close to copper material [2].

1.2.7 Donor and acceptor ionization energy level

In the silicon, donor and acceptor ionization energy is small, which allows the entire donor and acceptor impurities to be ionized at room temperature as well as at high temperatures. In silicon carbide, donor and acceptor impurities are not ionized at room temperature.

1.2.8 3C-SiC Structure

The notation used for the polytypes of SiC has certain physical significance depending upon the periodicity of stacking [16]. In 3C-SiC structure, ‘3’ means it has three bilayer periodicity and alphabet ‘C’ denotes cubic symmetry (Figure 1.10).

Figure 1.10. 3C-SiC structure [16].
The SiC material has stable chemical bond. The thermal expansion coefficient of SiC is very low \((4.06 \times 10^{-6} /K)\), which causes no phase distortion [16].

### 1.3 Fabrication Techniques

3C-SiC micro pillar arrays were fabricated on the silicon substrate by using the method of chemical vapor deposition (CVD). 3C-SiC micropillar arrays were selectively grown in the circular features via the vapor-liquid-solid (VLS) process [17]. Silane \((\text{SiH}_4)\) and acetylene \((\text{C}_2\text{H}_2)\) were used as source gases for fabrication of 3C-SiC on Si substrate.

The growth of 3C-SiC on Si has lots of advantages, such as low cost and large-size substrates. The main hurdles to the development of 3C-SiC on Si substrates are the lattice mismatch and large thermal expansion difference between silicon and silicon carbide, which often generates the defects such as twins, stacking faults and dislocations [17]. In order to overcome the difficulties, different methods were followed to grow 3C-SiC on Si. One of the promising techniques is called the flash lamp process [17]; vapor-liquid-solid process to grow 3C-SiC on silicon is popular compared to all other methods.

The VLS process is a general technique to grow single-crystal SiC nano-whiskers [18-19].
The growth of epi-layers involves the dissolution of solute at the vapor liquid interface and resultant precipitate at the liquid-solid interface. During the VLS growth process, silane (SiH$_4$) and acetylene (C$_2$H$_2$) were used as source gases; the growth temperature is around the 1200$^\circ$C [20]. Methane is also used as source gas but temperature required to grow 3C-SiC on silicon substrate is around 1350$^\circ$C. From this, different source gases are used to grow 3C-SiC on silicon wafer; C$_2$H$_2$ is more active than methane and propane.

The growth of 3C-SiC micro-pillars on Si wafer are carried out using a homemade cold-wall chemical vapor deposition (CVD) reactor [17]. This reactor is made with quartz tubes. The samples were held on a SiC-coated graphite susceptor which is inductively heated by radio frequency induction. Pyrometer with Pt-Rh thermocouple is used to monitor and control the temperature of a silicon substrate. Flow meters are used to control the gas flow rate.
The growth temperature of 3C-SiC was between 1150°C to 1200°C according to the Ni-Si and Ni-C phase diagrams. In this process, hydrogen is used as a carrier gas, which is purified by a Pd purifier. Hydrogen flow rate was 500 SCCM (standard cubic centimeters per minute). Silane and acetylene were used as source gases. Their flow rates were 3 and 2 SCCM respectively. The total pressure rate and growth time were 60 torr and 60 mins respectively.

The circular features show that the relative percentage of C, Si and Ni are 36%, 43%, and 21%, respectively. The EDS analysis shows that out-of- circular features indicates that the relative atomic percentage of C, Si and Ni are 42%, 54%, and 4%, respectively. From these results, circular features are covered by Ni-SiC droplets while those out-of- circular features are covered by SiC thin films.

From the Figure, 1.12 XRD results show the plot of intensity VS 2 theta-omega. From the Figure 1.12 the 3C-SiC (111) plane appears at 35.68°. No other XRD peaks from SiC polytypes are detected except those from 3C-SiC. Si(200) peak appears at 32.5°.
Figure 1.12. XRD plots of SiC micro pillar arrays [15].

From the Figure 1.13, it shows the SEM results; it is obvious that SiC micro pillars are grown with metallic Ni as catalyst. The growth rate of micro pillars in the circular features filling the catalyst is much higher than that of the thin film outside the feature without catalyst because catalyst increases the rate of reaction.
Figure 1.13 SEM image cross sectional view: (a) silicon carbide micro-pillars, and (b) silicon carbide micropillar on silicon substrate [17].

The EDS analysis of a single micro pillar shows that the relative percentage of the Si, C, Ni are 48.5%, 51.0%, and 0.5% respectively. The results show that in the central part of the...
micro pillar of Si/C it is a good composite with a little amount of Ni doped into the SiC micro pillar. 3C-SiC can be grown on Si (100) substrate by alternating epitaxy method at 1000°C.

The 3C –SiC was grown on Si substrate in a hot-wall low-pressure chemical vapor deposition reactor, with silane and acetylene, are being employed as precursors. Silicon substrate contamination is avoided by filling the reactor with oxygen to grow silicon dioxide, and the oxide layer was etched away by silane [20], followed by a carbonization step performed at 750°C [20]. The growth rate of 3C-SiC can be controlled by adjusting the supply volume of SiH₄ and C₂H₂ [20].

The most commonly used method to grow 3C-SiC on a silicon substrate is low-pressure chemical vapor deposition (LPCVD) by simultaneous sending of Si-containing and carbon-containing sources, diluted by H₂ [20]. The growth of 3C-SiC using LPCVD can be achieved at substrate temperature around 1350°C or higher [20], at which silicon melts and causes redistribution of dopents in silicon substrate and thermal mismatch between SiC/Si heterostructure.

Great efforts were made to find an alternative method, by utilizing the alternating supply or atomic layer epitaxy method. The growth temperature was reduced to1000°C for both hetero- and homo–epitaxial growth of 3C-SiC. This method consists of gas source molecular beam epitaxy (MBE) and LPCVD reactor [20]. With this process, thermal mismatch and wafer bowing is reduced. Due to MBE reactor being used for growth of 3C-SiC, ultra-high vacuum range between 10⁻⁴ and 10⁻³ Pa is used, (the investigated Si-containing source was disilane (Si₂H₆), and the carbon-containing sources were acetylene (C₂H₂) and propane (C₃H₈)). The MBE reactor is much more expensive and complex compared to LPCVD reactor [20].
The growth of 3C-SiC on Si is fabricated at low temperature by using dichlorosilane (SiH₂Cl₂) and C₂H₂ in a LPCVD reactor. At the temperature range of 750-1050°C [20], it is obvious that involvement of the H₂ was necessary to reduce SiH₂Cl₂ to enable the absorption of Si atoms on the surface of the carbonized substrate.

With the intermittent flow of H₂, a growth of single-crystalline 3C-SiC was observed [20]. With the continuous flow of H₂ poly crystalline 3C-SiC was grown. As a consequence, this process makes it complicated to control.

Heteroepitaxial growth of 3C-SiC on 150 mm Si (100) substrate by alternating supply epitaxy (ASE) using silane and acetylene as precursors. In this process, 3C-SiC film is grown on Si substrate in a hot-wall horizontal custom-made LPCVD reactor. The growth was performed at 1000°C with SiH₄ (99.4%) and C₂H₂ as precursors [20].

Initially, silicon (Si) substrate was cleaned prior to being loaded into the LPCVD reactor. The ideal temperature of the reactor was set at 600°C; after loading the Si into the reactor, temperature ramped from 600 to 1000°C (ramp rate 5°C /min) in the presence of oxygen at a pressure of 30 Pa. The goal of this process is to grow silicon dioxide to avoid the contamination of Si substrate by possible carbon-related residues in the reactor chamber. Next, the chamber was degassed for 30 sec and SiH₄ (flow rate 1.5 SCCM) for 15 mins to remove the silicon dioxide and then deposit the new Si layer on silicon substrate. After that, the temperature cooled down to 750°C in a vacuum then a flow of C₂H₂ (10 SCCM) at a pressure of 2 Pa was introduced into substrate to convert Si in to SiC from 750-900°C, followed by an increase in temperature from 900 to 1000°C with continued flow of C₂H₂ at a pressure of 40Pa then 3C-SiC, which was
formed cycle by cycle using the ASE method [20]. Each cycle consists of four steps: (i) the supply of SiH₄ with 10 to 60 sec with flow rate in the range of 0.3 to 2.5 SCCM, (ii) pump out for 5 to 30 sec, (iii) the supply of C₂H₂ for 5 to 120 sec with flow rate in the range of 0.8 to 10 SCCM, and (iv) pump out for 5 to 30 sec [20].

1.4 Proposed Fabrication Process

Figure 1.14 shows the proposed fabrication process for the vertical one-directional 3C-SiC MESFET. The first step in this process is to deposit silicon dioxide (SiO₂) or polyimide film on the n+(111) silicon substrate. This silicon dioxide acts as an insulator for silicon substrate. The total wafer is placed in the SiC growth reactor to grow the 3C-SiC pillars. The growth can be done using silane (SiH₄) and acetylene (C₂H₂) with a flow rate of 2 and 3 SCCM, respectively, at a reactor pressure of 60 torr and growth temperature between 1150°C and 1200°C [21].

After the 3C-SiC growth is finished, Ni metal etched away, and Schottky metal for the gate is deposited by using titanium metal. The part of the Schottky metal is etched to expose the drain surface areas. SiO₂ or polyimide is deposited to fill the volume between the devices [21]. The holes are etched and filled with metal to connect the gate electrode to outside connections. The final step is drain, and source metals are deposited.
1.5 Advantages

1.5.1 Advantages of 3C-SiC silicon carbide

- 3C-SiC can be easily grown on a large area of silicon substrate.
- 3C-SiC has higher mobility compared to silicon.
- 3C-SiC can be easily integrated with silicon.
- The high critical electric field (E_C) of 3C-SiC allows higher doping and thinner drift regions, thereby reducing the specific on-resistance (R_{on}) of power devices by over 2 orders of magnitude compared to silicon.
3C-SiC has a high value of electron saturation velocity and bulk mobility which make it suitable for high-frequency applications and reduces the mean power losses.

3C-SiC has an energy band gap that is almost three times that of silicon.

3C-SiC have avalanche/breakdown field and thermal conductivity that are 6 times and 3 times that of corresponding values of silicon.

3C-SiC is an attractive choice for power devices from a commercialization viewpoint. 3C-SiC films deposited on Si wafers could be utilized for a number of other potential applications including smart power devices and superior micro-electro-mechanical systems.

### 1.5.2 Advantages of vertical structure:

- The drain current of vertical MESFET is double that of the lateral structure with the same gate length and width.
- It can be cooled easily compared to lateral structures.
- Devices can be connected in parallel in order to get higher currents.
- Vertical structure occupies lowest area compared to that of lateral structures so that heat sink area is reduced, and the cost of the device is also reduced.
- The vertical device covers only 33% of the area covered by lateral structure device.
- Vertical structure can provide low stress capacitances.

### 1.6 Objective of the thesis

The objective of this thesis is to design a vertical one-directional 3C-SiC MESFET on the silicon substrate model. The model is then used to study the device’s electrical characteristics.
using Silvaco Atlas software. This model is also used to investigate the thermal behavior using COMSOL Multiphysics.

1.7 Thesis Organization

Chapter 2 details the modeling of the one-directional 3C-SiC MESFET on silicon substrate using Silvaco Atlas software. Chapter 3 discusses the thermal behavior of the device using COMSOL Multiphysics software. In Chapter 4, the simulation results from the model are discussed. In Chapter 5, conclusions are drawn, and future research is proposed.
CHAPTER 2

ELECTRICAL STUDY OF ONE-DIRECTIONAL 3C-SiC VERTICAL MESFET ON SILICON SUBSTRATE

2.1 Introduction of silvaco atlas software

Device modeling using simulation enables quick design, test and evaluation of semiconductor devices without fabricating them. These result in huge advantages in terms of cost reduction and vastly reduced time to market. It is possible to study different device structures in a very short time. Simulation tools are often used to obtain device performance parameters such as potential, carrier and current profile within the device during operation, which is not measured experimentally.

The simulation software package used in this thesis work is a commercial semiconductor device simulation Atlas from Silvaco Inc. Semiconductor device design is much easier in Silvaco atlas software. Some of the major tools that are included in this package are Athena, Deckbuild, and Tonyplot, etc [22]. Devices are built-in Deckbuild, simulations are run in Atlas, and output can be seen in Tonyplot.

Silvaco Atlas is a versatile, extendable software product for two and three-dimensional device simulation. The equation that describes the operation of a device in two-dimensional grids consists of a large number of grid points called nodes. The Atlas simulation totally depends on physics-based models such as carrier generation, recombination and transportation that are responsible for the operation of the device [23].
Atlas solves three fundamental equations when simulating a power semiconductor device: Poisson’s equation, transport equation and continuity density to electrostatic potential, which allows the calculation of electric fields. Depending upon the potential for most of the application drift diffusion, transport equations are used [23].

2.2 Semiconductor device design procedure in Silvaco Atlas software

Figure 2.1 shows the basic semiconductor device design in Silvaco Atlas software. Initially, mesh is created with appropriate dimensions. After creating the mesh, it is divided into different sections called regions. The user can specify the electrodes for the device such as source, drain and gate electrodes. The user can specify the appropriate doping concentration for each region. If the user uses new material, it is important to mention the material and model properties. Silvaco Atlas software has some default material library if the user does not mention material properties. It will take default values, and silicon is the most widely used default semiconductor material. The next step is that the user must specify the contacts. If the contact is Schottky contact, it is important to mention the work function of the material. If the contact is ohmic contact, there is no need to mention the work function. Numerical selection is an important part in device design. The Newton method is simple to use; Gummel Newton method is also used to find a solution.
Figure 2.1. Semiconductor device design procedure in Silvaco Atlas software.
2.3 Proposed device structure

From the Figure 2.2 and 2.3 it shows a proposed one-directional normally-on 3C-SiC MESFET on the silicon substrate with a drain Schottky contact. The source ohmic contact is formed on $n^+$ silicon substrate. Titanium material is used as Schottky contact for gate and drain contact. Titanium is also used as an ohmic contact for source material. The choice of titanium is because it can withstand high temperatures [21]. The $n^+$-SiC formed on top of the silicon substrate; on top of this layer $n$-SiC is channel grown. The titanium metal contact on top of this layer forms the drain contact.

This total structure forms one-directional 3C-SiC MESFET, where current can only flow from drain to source, as it will be blocked by the drain contact if the drain-source voltage is reversed. This structure will block any unwanted current that may flow from source to drain due to the fault in the circuit [21]. The layers of doping are $10^{21}$ for the $n^+$ Si substrate, $10^{21}$ cm$^{-3}$ for the $n^+$ SiC, and $10^{17}$ cm$^{-3}$ for n-SiC for the channel layer. The default width of the device is taken as 1$\mu$m.
Figure 2.2. Structure of one-directional normally-on 3C-SiC MESFET [21].

Figure 2.3. Top view of a one-directional normally-on 3C-SiC MESFET.
2.4 Proposed Device Simulation

Numerical simulation of the device performed using Silvaco Atlas software. The structure shown in Figure 2.2 was built-in the program. The device has the following dimensions: gate length is 0.5\(\mu\)m, gate width is 1\(\mu\)m, a space between the gate and source is 6.25\(\mu\)m, and channel thickness is 0.5\(\mu\)m [21]. It should be noted that the device has double channel with double depletion regions at both sides [21]. The work function of 4.33 V for titanium is used as the Schottky contact.

\[ V_T = V_{bi} - V_{po} \quad (2.1) \]

\[ V_{po} = \frac{qN_D a^2}{2\varepsilon} \quad (2.2) \]

where:

- \(V_T\) is the threshold voltage
- \(V_{bi}\) is the built-in potential
- \(V_{po}\) is the pinch-off voltage
- \(N_D\) is the doping concentration of channel
- \(a\) is the channel thickness
- \(\varepsilon\) is the permittivity of 3C-SiC material

The theoretical built-in potential, pinch-off voltage, threshold voltage, drain current and critical breakdown electric field were calculated using MATHCAD software. Threshold voltage, drain voltage Vs drain current, breakdown voltage, critical electric field were found using Silvaco Atlas software. The threshold voltage of the device using Silvaco atlas is -5.25V and drain current is 0.6 mA. The breakdown voltage is 625V.
CHAPTER 3
THERMAL STUDY OF ONE-DIRECTIONAL NORMALLY-ON VERTICAL 3C-SiC MESFET ON SILICON SUBSTRATE USING COMSOL SOFTWARE

3.1 Introduction to COMSOL Multiphysics software

The COMSOL [24] Multiphysics simulation system represents a powerful tool for analysis of semiconductor devices. It uses a heat field of power electronic systems to allow one to obtain the information about temperature distribution; thereby it is easy to expose areas with the most thermal overload of an object before the appliance of the cooling system [25]. The semiconductor device function is guaranteed only at certain temperatures, at which the upper limit of temperature is of great importance. For a device based on silicon, the temperature ranges between 150-180°C [25], but for SiC technology can extend the temperature range from 300-340°C.

It is necessary to design a cooling system that serves to maintain the maximum temperature of the semiconductor material, and it is also necessary to have knowledge about the temperature decomposition for the whole device in order to protect other elements such as wiring network, capacitors, and inductors [25]. At present, designers use heat transfer by using the conduction technique. Its relative accuracy is low; therefore, it uses a large-sized cooling system.
The COMSOL Multiphysics was founded by Mr. Svante Littmarck and Mr. Farhad in 1986. It was initially developed in Sweden. Later on it has grown to the United Kingdom, U.S.A, China, India, and so on. At present, the COMSOL plays a vital role in science, research and engineering calculation. It uses the finite element method to solve the problem. The first version of COMSOL Multiphysics was published in 1998, and it was named Toolbox. In the beginning, it was applied in the field of structural mechanics. COMSOL Multiphysics facilitates all steps in the modeling process: geometry definition, specifying material properties, specifying physics, meshing, solving and results [24].

3.2 Heat transfer methods

The temperature is state variable; it determines an atom internal kinetic energy of material. Inside the material, the thermal energy is transferred from high temperature to low temperature. Heat transfer is performed in three ways:

3.2.1 Conduction

Conduction mainly applies to the solid state material. In conduction process, heat is transferred from a high-temperature region to a low-temperature region. The device side area $S$ $[m^2]$, thickness $d[m]$ and temperature difference $\Delta T$ [25]:

$$\Delta T = T_2 - T_1 (k)$$  \hspace{1cm} (3.1)

$$I_{\text{Conduction}} = ((S \cdot \lambda)/d) \Delta T$$  \hspace{1cm} (3.2)

where $\lambda$ is the heat conductivity of material.

The amount of heat conduction is

$$Q_{\text{Conduction}} = I_{\text{conduction}} \times t$$  \hspace{1cm} (3.3)

where $t$ is the time in seconds.
3.2.2 Convection

The convection takes place by passage of heat from a solid material to gaseous or fluid environment that is surrounded by solid material. There are two types of convection.

\[ I_{\text{Conduction}} = K \cdot S \cdot \Delta T \]  \hspace{1cm} (3.4)

where:

- \( K \) is the index of heat transfer
- \( S \) is surface area
- \( \Delta T \) is temperature difference.

3.2.2.1 Straight line flow

Straight line flow occurs when the speed of fluid flow is slow, uniform and encapsulated in the area of the flow of the material.

3.2.2.2 Turbulent flow

Turbulent flow occurs when the speed of fluid is high. It causes the mutual shuffle of particles in the cooling medium, whereby there is a mutual handover between molecules of the cooling medium [25].

3.2.3 Radiation

In general, every material that has a higher temperature than absolute zero becomes the source of radiation. It is accomplished through vibration. After the impact of energy of vibration on the body, it turns into heat. The following three cases occurred.

In the first case thermal radiation is released through the body. Heat permeability \( \alpha \) depends on the material from which body is made, and wave length of thermal radiation. In the second case, part of the radiation is reflected from the body. Radiation depends on the material
from which the body is made and the structure of the body, and it is represented by $\sigma$. In the final case, part of the thermal radiation is absorbed by the body. The thermal radiation depends on the color of the body; it is represented by $\gamma$. The following equation shows total captured energy [25]:

$$\gamma + \sigma + \alpha = 1$$

A three-dimensional finite element model was developed to simulate the thermal behavior of the vertical one-directional 3C-SiC MESFET using COMSOL Multiphysics.

The heat conduction in solids is given by following equation:

$$\rho \cdot C_p \frac{dT}{dt} - \nabla (K \nabla T) = Q$$

where:

$\rho$ is the density (Kg/m$^3$)

$C_p$ is the heat capacity (J/KgK)

$K$ is the thermal conductivity (W/mK)

$Q$ is the heat source (watt)

$T$ is the temperature (K)

3.3 Device design in COMSOL Multiphysics Software:

COMSOL Multiphysics is a powerful interactive program which presents a modeling environment. (Figure 3.1) It solves a lot of engineering and scientific problems effectively by using partial differential equations (PDE); this software is not only applicable to single physics applications but also applies to multiphysics applications.
The COMSOL Multiphysics environment contains physical models based on partial differential equations. In each model, the user can select material from material library, or the user can add new material properties to the library. COMSOL can process the modified differential equation without a programmer’s detailed knowledge about mathematics and numerical analysis. Mathematical application modes of COMSOL Multiphysics modules perform different types of analysis like stationary and time-dependent study analysis, linear and non-linear analysis, etc.

It uses a finite element method for numerical analysis. It is suitable for various application fields like acoustics, semiconductors, heat transfer, and structural mechanics applications, etc.
COMSOL uses environment that contains different geometry shapes like rectangles, cubes, blocks, cones, cylinders, spheres, polygons and ellipsoids, etc. The user can import the geometric shape from a CAD tool and control the mesh by customizing the mesh by parameters of a mesh driver. COMSOL can solve stationary and transient studies.

3.4 Proposed structure in COMSOL multiphysics (Figure 3.2)

Figure 3.2 Proposed structure in COMSOL
CHAPTER 4
RESULTS AND ANALYSES

This chapter discusses the results obtained by the electrical and thermal models discussed in Chapters 2 and 3. The electrical model calculates drain current, threshold voltage, critical electric field, and breakdown voltage. The thermal model calculates the temperature of the device for various drain voltages and heat flux coefficient values. This chapter also discusses the temperature effect on device parameters, and doping concentration effect on device parameters. It is also investigating the effect of drain voltage, power, and heat flux coefficient values on temperature of the device.

Figure 4.1 shows the drain current of vertical 3C-SiC one-directional MESFET at different temperatures. Figure 4.1(a), shows the drain current at 300K was 0.6 mA obtained for a gate voltage of 0 V and drain voltage of 20V. Figure 4.1(b), shows the drain current at 450K was 0.35 mA obtained for a gate voltage of 0 V and drain voltage of 20V. From Figure 4.1(c), it shows the drain current at 600K was 0.22 mA obtained for a gate voltage of 0 V and drain voltage of 20V. Figure 4.1(d), shows the drain current at 750K was 0.16 mA obtained for a gate voltage of 0 V and drain voltage of 20V. Figure 4.1(e), shows the drain current at 900K was 0.12 mA obtained for a gate voltage of 0 V and drain voltage of 20V. As the temperature increased from 300 K to 900K, drain current value decreased. As the drain voltage increased from 0 V to 20 V, the drain current increased due to the short channel effect.
Figure 4.1. Drain voltage vs drain current plots at a temperature of (a) 300K, (b) 450K, (c) 600K, (d) 750K, and (e) 900K. Gate voltages from top are 0V, -1.5V, -2.5V, -3.5V, -4.5V, -5.5V.
Figure 4.2 shows the vertical 3C-SiC one-directional MESFET threshold voltage characteristics at various temperatures, with fixed drain voltage of 20V. Threshold voltage of the device at 300K was -4.75V. As the temperature increases, threshold voltage maintains constant because silicon carbide is a wide band gap semiconductor, and there is no significant increase in carrier concentration taking place due to a rise in temperature.

\[ V_T = V_{bi} - V_{po} \]  
\[ V_{po} = \frac{qN_D a^2}{2\varepsilon} \]  

Figure 4.3 shows the breakdown voltage of vertical 3C-SiC one-directional MESFET for various temperatures. At 300K, a gate voltage of 0 V and breakdown voltage of the device is 625 V. As the temperature of the device increases from 300K to 900 K, breakdown voltage remains constant. Due to the fact that 3C-SiC is a wide band gap semiconductor, its carrier concentration does not change with the rise in temperature.

\[ R_{on-sp} = \frac{4\varepsilon \nu^2}{\varepsilon_{\mu_n} E_c^3} \]  

From Figure 4.4, electric field is plotted for fixed gate voltage of 0 V and different drain voltages. Figure 4.4(a) shows the maximum breakdown electric field is 3.9x10^6 V/cm for the drain voltage of 625V, and most of the electric field concentrated near gate edges. The width of the depletion region is 0.15 microns. Figure 4.4(b) shows the critical breakdown electric field of the device for drain voltage of 500 V is 3.61x10^6 V/cm; critical breakdown electric field starts near the gate edges, and depletion width is 0.15 microns. Figure 4.4(c) shows the critical breakdown electric field for drain voltage of 400V is 3.31x10^6 V/cm, with most of the electric field concentrated near the gate edges, and the depletion width is 0.15 microns.
Figure 4.2. Threshold voltage of device at a temperature of (a) 300K, (b) 450K, (c) 600K, (d) 750K, and (e) 900K.
Figure 4.3 Breakdown voltage of device at a temperature of (a) 300K, (b) 450K, (c) 600K, (d) 750K, and (e) 900K. Gate voltages from top are 0V, -1.5V, -3V, -4V, -5V.
Figure 4.4. Electric field of device for gate voltage of 0 V: (a) drain voltage of 625 V, (b) drain voltage of 500 V, (c) drain voltage of 400 V, (d) drain voltage of 300 V, (e) drain voltage of 200 V, and (f) drain voltage of 100 V.
Figure 4.4(d) shows the maximum electric field for the device at drain voltage of 300V is 2.96x10^6 V/cm, with most of the electric field concentrated near gate edges, and the depletion width is 0.15 microns.

Figure 4.4(e) shows that the maximum electric field of the device for drain voltage of 100V is 2.53x10^6 V/cm, with maximum electric field concentrated near gate edges, and the depletion width is 0.15 microns. Figure 4.4(f) shows the maximum electric field for the device for drain voltage of 300V is 1.84x10^6 V/cm; most of the electric field is concentrated near gate edges, and the depletion width is 0.15 microns.

From Figure 4.5, electric field is plotted for fixed gate voltage of -1.5V and various drain voltages. Figure 4.5(a) shows the maximum electric field is 4.23x10^6 V/cm for drain voltage of 625V, and most of the electric field concentrated near gate edges; and depletion width is 0.2 microns. Figure 4.5(b) shows the critical breakdown electric field of the device for drain voltage of 500 V is 3.94x10^6 V/cm; critical breakdown electric field starts near the gate edges, and depletion width is 0.2 microns. Figure 4.5(c) shows the critical breakdown electric field for drain voltage of 400V is 3.6x10^6 V/cm, with most of the electric field concentrated near the gate edges, and the depletion width is 0.2 microns. Figure 4.5(d) shows the maximum electric field for the device at drain voltage of 300V is 3.21x10^6 V/cm, with most of the electric field concentrated near gate edges, and the depletion width is 0.2 microns. Figure 4.5(e) shows the maximum electric field of the device for drain voltage of 200V is 2.75x10^6 V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.2 microns. Figure 4.5(f) shows the maximum electric field of the device for drain voltage of 100V is 1.85x10^6 V/cm, with maximum electric field concentrated near gate edges.
Figure 4.5. Electric field of device for gate voltage of -1 V: (a) drain voltage of 625 V, (b) drain voltage of 500 V, (c) drain voltage of 400 V, (d) drain voltage of 300 V, (e) drain voltage of 200 V, and (f) drain voltage of 100 V.
For Figure 4.6, electric field is plotted for fixed gate voltage of -2.5V and various drain voltages. Figure 4.6(a) shows the maximum electric field is $4.49 \times 10^6 \text{ V/cm}$.

Figure 4.6(b) shows the critical breakdown electric field of the device for drain voltage of 500 V is $4.19 \times 10^6 \text{ V/cm}$; critical breakdown electric field starts near the gate edges, and depletion width is 0.23 microns. Figure 4.6(c) shows the critical breakdown electric field for drain voltage of 400V is $3.83 \times 10^6 \text{ V/cm}$, with most of the electric field concentrated near the gate edges, and the depletion width is 0.23 microns. Figure 4.6(d) shows the maximum electric field for the device at drain voltage of 300V is $3.41 \times 10^6 \text{ V/cm}$, with most of the electric field concentrated near gate edges, and the depletion width is 0.23 microns. Figure 4.6(e) shows the maximum electric field of the device for drain voltage of 200V is $2.92 \times 10^6 \text{ V/cm}$, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.23 microns. Figure 4.6(f) shows the maximum electric field of the device for drain voltage of 100V is $1.96 \times 10^6 \text{ V/cm}$, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.23 microns. At drain voltage 100V, the depletion region starts from drain end; as the drain voltage increases from 100V to 625V, most of the channel depleted under the gate.

From Figure 4.7, electric field is plotted for fixed gate voltage of -3.5V and various drain voltages. Figure 4.7(a) shows the maximum electric field is $4.72 \times 10^6 \text{ V/cm}$ for drain voltage of 625V; and most of the electric field is concentrated near gate edges, and depletion width is 0.24 microns. Figure 4.7(b) shows the critical breakdown electric field of the device for drain voltage of 500 V is $4.39 \times 10^6 \text{ V/cm}$; critical breakdown electric field starts near the gate edges, and depletion width is 0.24 microns.
Figure 4.6 Electric field of device for gate voltage of -2 V: (a) drain voltage of 625 V, (b) drain voltage of 500 V, (c) drain voltage of 400 V, (d) drain voltage of 300 V, (e) drain voltage of 200 V, and (f) drain voltage of 100 V.
Figure 4.7 Electrical field for the device for gate voltage -3V: (a) drain voltage of 625 V, (b) drain voltage of 500 V, (c) drain voltage of 400 V, (d) drain voltage of 300 V, (e) drain voltage of 200 V, and (f) drain voltage of 100 V.
Figure 4.7(c) shows the critical breakdown electric field for drain voltage of 400V is 4.17x10^6 V/cm, with most of the electric field concentrated near the gate edges, and the depletion width is 0.24 microns. Figure 4.7(d) shows the maximum electric field for the device at drain voltage of 300V is 3.58x10^6 V/cm, with most of the electric field concentrates near gate edges, and the depletion width is 0.24 microns. Figure 4.7(e) shows the maximum electric field of the device for drain voltage of 200V is 3.07x10^6 V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.24 microns. Figure 4.7(f) shows the maximum electric field of the device for drain voltage of 100V is 2.07x10^6 V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.24 microns. At drain voltage 100V, the depletion region starts from drain end; as the drain voltage increases from 100V to 625V, most of the channel depleted under the gate.

In Figure 4.8, electric field is plotted for fixed gate voltage of -4.5V and various drain voltages. Figure 4.8(a) shows the maximum electric field is 4.9x10^6 V/cm for drain voltage of 625V; and most of the electric field is concentrated near gate edges, and depletion width is 0.25 microns. Figure 4.8(b) shows the critical breakdown electric field of the device for drain voltage of 500 V is 4.56x10^6 V/cm; critical breakdown electric field starts near the gate edges, and depletion width is 0.25 microns. Figure 4.8(c) shows that the critical breakdown electric field for drain voltage of 400V is 4.17x10^6 V/cm, with most of the electric field concentrated near the gate edges, and the depletion width is 0.25 microns. Figure 4.8(d) shows the maximum electric field for the device at drain voltage of 300V is 3.72x10^6 V/cm, with most of the electric field concentrated near gate edges, and the depletion width is 0.25 microns.
Figure 4.8 Electric field of device for gate voltage of -4V: (a) drain voltage of 625V, (b) drain voltage of 500V, (c) drain voltage of 400V, (d) drain voltage of 300V, (e) drain voltage of 200V, and (f) drain voltage of 100V.
Figure 4.8(e) shows the maximum electric field of the device for drain voltage of 200V is $3.19 \times 10^6$ V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.25 microns. Figure 4.8(f) shows the maximum electric field of the device for drain voltage of 100V is $2.16 \times 10^6$ V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.25 microns.

In Figure 4.9, electric field is plotted for fixed gate voltage of -5.5V and various drain voltages. Figure 4.9(a) shows the maximum electric field is $5.07 \times 10^6$ V/cm for drain voltage of 625V; and most of the electric field is concentrated near gate edges, and depletion width is 0.35 microns. Figure 4.9(b) shows the critical breakdown electric field of the device for drain voltage of 500 V is $4.72 \times 10^6$ V/cm; critical breakdown electric field starts near the gate edges, and depletion width is 0.35 microns. Figure 4.9(c) shows the critical breakdown electric field for drain voltage of 400V is $4.31 \times 10^6$ V/cm, with most of the electric field concentrated near the gate edges, and the depletion width is 0.35 microns. Figure 4.9(d) shows the maximum electric field for the device at drain voltage of 300V is $3.3 \times 10^6$ V/cm, with most of the electric field concentrated near gate edges, and the depletion width is 0.35 microns. Figure 4.9(e) shows the maximum electric field of the device for drain voltage of 200V is $3.19 \times 10^6$ V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.25 microns. Figure 4.9(f) shows the maximum electric field of the device for drain voltage of 100V is $2.24 \times 10^6$ V/cm, with maximum electric field concentrated near gate edges, and the maximum depletion width is 0.35 microns. At drain voltage 100V, the depletion region starts from drain end; as the drain voltage increases from 100V to 625V, most of the channel depleted under the gate.
Figure 4.9 Electric field of device for gate voltage of -5 V: (a) drain voltage of 625V, (b) drain voltage of 500V, (c) drain voltage of 400V, (d) drain voltage of 300 V, (e) drain voltage of 200V, and (f) drain voltage of 100V.
4.1 Effect of Temperature on Device Characteristics

The values of device parameters as a function of temperature are plotted in Figure 4.10. From Table 4.1 and Figure 4.10(a) it is observed that as the temperature increases from 300K to 900 K, the threshold voltage of the device remains constant because there is no significant increase in the carrier’s concentration. This takes place due to rise in temperature. From Figure 4.10(b) it is observed that as the temperature increases from 300K to 900K, the drain current decreases due to decrease in mobility equation. From the equation 4.4, the semiconductor device current not only depends on doping concentration but also mobility. As temperature increases, mobility decreases and due to this, drain current decreases. From Figure 4.10(c) it is observed that as the temperature increases from 300K to 900K, breakdown voltage of the device remains constant because there is no significant increase in carrier concentration due to an increase in temperature.

\[ I = qN_D\mu_n \]  \hspace{1cm} (4.4)

where:

I is the current (A)

N_D is the donor doping concentration (cm^{-3})
Figure 4.10 Temperature plots: (a) temperature versus threshold voltage, (b) temperature versus drain current, (c) temperature versus breakdown voltage.

Table 4.1 EFFECT OF TEMPERATURE ON DEVICE CHARACTERISTICS

<table>
<thead>
<tr>
<th>Temperature (k)</th>
<th>Threshold voltage (v)</th>
<th>Drain current (mA)</th>
<th>Breakdown voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>-4.75</td>
<td>0.6</td>
<td>625</td>
</tr>
<tr>
<td>450</td>
<td>-4.75</td>
<td>0.35</td>
<td>625</td>
</tr>
<tr>
<td>600</td>
<td>-4.75</td>
<td>0.22</td>
<td>625</td>
</tr>
<tr>
<td>750</td>
<td>-4.75</td>
<td>0.16</td>
<td>625</td>
</tr>
<tr>
<td>900</td>
<td>-4.75</td>
<td>0.12</td>
<td>625</td>
</tr>
</tbody>
</table>
4.2 Effect of Doping Concentration on Device Characteristics

The values of device parameters are plotted as a function of doping concentration in Figure 4.11. From Figure 4.11(a), it is observed that as the doping concentration increases, drain current increases up to a certain extent and starts decreasing. This can be attributed to the fact that drain current not only depends on doping concentration but also depends on mobility of carriers. From the equation 4.4(a), as the doping concentration increases, current increases.

From Figure 4.11(b), as the doping concentration increases, threshold voltage decreases. This can be attributed to the fact that as the doping concentration increases, pinch-off voltage increases from equation 4.1. Threshold voltage is the difference between built-in potential and pinch-off voltage. The built-in potential is taken as \( \frac{2}{3}E_g \) and this value is fixed. Threshold voltage is changes with pinch-off voltage. As the pinch-off voltage increases, threshold voltage goes into more negative voltage.

\[
V_{po} = \frac{qNDa^2}{2\varepsilon} \quad (4.5)
\]

\[
V_T = V_{bi} - V_{po} \quad (4.6)
\]

where:

- \( V_{bi} \) is the built-in potential
- \( V_{po} \) is the pinch-off potential
- \( V_T \) is the threshold voltage
- \( a \) is the channel thickness
- \( N_D \) is the donor doping concentration
- \( \varepsilon \) is the permittivity of 3C-SiC material
From Figure 4.11(c), as the doping concentration increases, breakdown voltage starts to decrease (Table 4.2). This can be explained with equations 4.3 and 4.4. From equation 4.3, as the doping concentration increases, specific on-resistance decreases due to a decrease in specific on-resistance; in Equation 4.4, the breakdown voltage decreases.

\[ R_{on-sp} = \frac{W_{pp}}{q\mu_n N_D} \]  \hspace{1cm} (4.7)

\[ R_{on-sp} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3} \]  \hspace{1cm} (4.8)

where:

- \( W_{pp} \) is the width of the depletion region
- \( \mu_n \) is the mobility of electrons
- \( N_D \) is the donor doping concentration
- \( BV \) is the breakdown voltage
- \( E_C \) is the critical electric field
- \( \varepsilon_s \) is the permittivity of 3C-SiC material
- \( R_{on-sp} \) is the specific on-resistance
Figure 4.11 Doping concentration plots: (a) doping concentration versus current, (b) doping concentration versus threshold voltage, and (c) doping concentration versus breakdown voltage.

Table 4.2 EFFECT OF DOPING CONCENTRATION ON DEVICE CHARACTERISTICS

<table>
<thead>
<tr>
<th>Doping concentration</th>
<th>Threshold voltage (v)</th>
<th>Drain current(mA)</th>
<th>Breakdown voltage (v)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$8 \times 10^{16}$</td>
<td>-5</td>
<td>0.48</td>
<td>650</td>
</tr>
<tr>
<td>$1 \times 10^{17}$</td>
<td>-4.75</td>
<td>0.6</td>
<td>625</td>
</tr>
<tr>
<td>$2 \times 10^{17}$</td>
<td>-12.5</td>
<td>1.25</td>
<td>575</td>
</tr>
<tr>
<td>$3 \times 10^{17}$</td>
<td>-18</td>
<td>1.6</td>
<td>540</td>
</tr>
<tr>
<td>$4 \times 10^{17}$</td>
<td>-25</td>
<td>2.4</td>
<td>475</td>
</tr>
<tr>
<td>$5 \times 10^{17}$</td>
<td>-30</td>
<td>2.75</td>
<td>460</td>
</tr>
<tr>
<td>$6 \times 10^{17}$</td>
<td>-36</td>
<td>3.2</td>
<td>450</td>
</tr>
</tbody>
</table>
4.3 Effect of Drain voltage on Device Electric field

Electric field of the device is found out for different drain voltages for fixed gate voltages such as 0V, -1V, -2V, -3V, -4V, -5V and plotted in Table 4.3 and Figure 4.12. From Figure 4.12(a), electric field of the device is found for fixed gate voltage of 0V and different drain voltages. The maximum electric field of the device is $3.9 \times 10^6$ V/cm, and it is obtained for the drain voltage of 625V. The minimum electric field of the device is $1.68 \times 10^6$ V/cm, and it is obtained for drain voltage of 100V. As the drain voltage increases from 100V to 625V, the electric field of the device increases. This is due to the direct relation between electric field and drain voltage.

Velocity of the carriers is given by the following relations:

$$V_s = \mu E \quad (4.9)$$

$$E = \frac{V_{ds}}{L} \quad (4.10)$$

$$V_s = \frac{\mu V_{ds}}{L} \quad (4.11)$$

where:

- $V_s$ is the velocity of carriers
- $\mu$ is the mobility of carriers
- $E$ is the electric field
- $V_{ds}$ is the drain to source voltage
- $L$ is the gate length.
Figure 4.12 Electric field of device versus Drain voltage for (a) gate voltage of 0 V, (b) gate voltage of -1 V, (c) gate voltage of -2 V, (d) gate voltage of -3 V, (e) gate voltage of -4 V, and (f) gate voltage of -5 V.
Table 4.3 EFFECT OF DRAIN VOLTAGE ON THE DEVICE ELECTRIC FIELD FOR 0V GATE VOLTAGE

<table>
<thead>
<tr>
<th>Gate voltage (V)</th>
<th>Drain voltage (v)</th>
<th>Electric field (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100</td>
<td>1.68x10^6</td>
</tr>
<tr>
<td>0</td>
<td>240</td>
<td>2.53x10^6</td>
</tr>
<tr>
<td>0</td>
<td>340</td>
<td>2.96x10^6</td>
</tr>
<tr>
<td>0</td>
<td>440</td>
<td>3.31x10^6</td>
</tr>
<tr>
<td>0</td>
<td>540</td>
<td>3.61x10^6</td>
</tr>
<tr>
<td>0</td>
<td>640</td>
<td>3.90x10^6</td>
</tr>
</tbody>
</table>

From Figure 4.12(b), the electric field of the device is found for fixed gate voltage of -1V and different drain voltages.

Table 4.4 EFFECT OF DRAIN VOLTAGE ON THE DEVICE ELECTRIC FIELD FOR -1V GATE VOLTAGE

<table>
<thead>
<tr>
<th>Gate voltage (v)</th>
<th>Drain voltage</th>
<th>Electric field (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>100</td>
<td>1.84x10^6</td>
</tr>
<tr>
<td>-1</td>
<td>240</td>
<td>2.75x10^6</td>
</tr>
<tr>
<td>-1</td>
<td>340</td>
<td>3.21x10^6</td>
</tr>
<tr>
<td>-1</td>
<td>440</td>
<td>3.60x10^6</td>
</tr>
<tr>
<td>-1</td>
<td>540</td>
<td>3.94x10^6</td>
</tr>
<tr>
<td>-1</td>
<td>640</td>
<td>4.23x10^6</td>
</tr>
</tbody>
</table>

From Figure 4.12(c), electric field of the device is found for fixed gate voltage of -2V and different drain voltages.
Table 4.5 EFFECT OF DRAIN VOLTAGE ON THE DEVICE ELECTRIC FIELD FOR -2V GATE VOLTAGE

<table>
<thead>
<tr>
<th>Gate voltage (v)</th>
<th>Drain voltage (v)</th>
<th>Electric field (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>100</td>
<td>1.96x10^6</td>
</tr>
<tr>
<td>-2</td>
<td>240</td>
<td>2.92x10^6</td>
</tr>
<tr>
<td>-2</td>
<td>340</td>
<td>3.41x10^6</td>
</tr>
<tr>
<td>-2</td>
<td>440</td>
<td>3.83x10^6</td>
</tr>
<tr>
<td>-2</td>
<td>540</td>
<td>4.19x10^6</td>
</tr>
<tr>
<td>-2</td>
<td>640</td>
<td>4.49x10^6</td>
</tr>
</tbody>
</table>

The maximum electric field of the device for drain voltage of 625V is 4.49x10^6 V/cm. The minimum electric field of the device is 1.96x10^6 V/cm, and it is obtained for drain voltage of 100V. From the equation 4.10, as the drain voltage increases from 100V to 625V, the electric field of the device increases. This is due to the fact that a direct relation exists between drain voltage and electric field.

From Figure 4.12(c), the electric field of the device is found for fixed gate voltage of -3V and different drain voltages.

Table 4.6 EFFECT OF DRAIN VOLTAGE ON THE DEVICE ELECTRIC FIELD FOR -3V GATE VOLTAGE

<table>
<thead>
<tr>
<th>Gate voltage (v)</th>
<th>Drain voltage (v)</th>
<th>Electric field (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3</td>
<td>100</td>
<td>2.07x10^6</td>
</tr>
<tr>
<td>-3</td>
<td>240</td>
<td>3.07x10^6</td>
</tr>
<tr>
<td>-3</td>
<td>340</td>
<td>3.58x10^6</td>
</tr>
<tr>
<td>-3</td>
<td>440</td>
<td>4.17x10^6</td>
</tr>
<tr>
<td>-3</td>
<td>540</td>
<td>4.39x10^6</td>
</tr>
<tr>
<td>-3</td>
<td>640</td>
<td>4.72x10^6</td>
</tr>
</tbody>
</table>

The maximum electric field of the device is 4.72x10^6 V/cm, and it is obtained for the drain voltage of 625V. The minimum electric field of the device is 2.07x10^6 V/cm, and it is obtained for the drain voltage of 100V. From equation 4.10, as the drain voltage increases from
100V to 625V, electric field of the device increases. This is due to the fact that a direct relation exists between drain voltage and electric field.

From Figure 4.12(d), the electric field of the device is found for fixed gate voltage of -4V and different drain voltages.

Table 4.7 EFFECT OF DRAIN VOLTAGE ON THE DEVICE ELECTRIC FIELD FOR -4V

<table>
<thead>
<tr>
<th>Gate voltage (v)</th>
<th>Drain voltage (v)</th>
<th>Electric field (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4</td>
<td>100</td>
<td>2.16x10^6</td>
</tr>
<tr>
<td>-4</td>
<td>240</td>
<td>3.19x10^6</td>
</tr>
<tr>
<td>-4</td>
<td>340</td>
<td>3.72x10^6</td>
</tr>
<tr>
<td>-4</td>
<td>440</td>
<td>4.17x10^6</td>
</tr>
<tr>
<td>-4</td>
<td>540</td>
<td>4.56x10^6</td>
</tr>
<tr>
<td>-4</td>
<td>640</td>
<td>4.90x10^6</td>
</tr>
</tbody>
</table>

The maximum electric field of the device is 4.90x10^6 V/cm, and it is obtained for the drain voltage of 625V. The minimum electric field of the device is 2.16x10^6 V/cm, and it is obtained for the drain voltage of 100V. From the equation 4.10, as the drain voltage increases from 100V to 625V, electric field of the device increases; this is due to the fact that a direct relation that exists between drain voltage and electric field.

From Figure 4.12(e), the electric field of the device is found for fixed gate voltage of -5V and different drain voltages.
Table 4.8 EFFECT OF DRAIN VOLTAGE ON THE DEVICE ELECTRIC FIELD FOR -5V GATE VOLTAGE

<table>
<thead>
<tr>
<th>Gate voltage (v)</th>
<th>Drain voltage (v)</th>
<th>Electric field (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5</td>
<td>100</td>
<td>2.20x10^6</td>
</tr>
<tr>
<td>-5</td>
<td>240</td>
<td>3.30x10^6</td>
</tr>
<tr>
<td>-5</td>
<td>340</td>
<td>3.85x10^6</td>
</tr>
<tr>
<td>-5</td>
<td>440</td>
<td>4.31x10^6</td>
</tr>
<tr>
<td>-5</td>
<td>540</td>
<td>4.72x10^6</td>
</tr>
<tr>
<td>-5</td>
<td>640</td>
<td>5.07x10^6</td>
</tr>
</tbody>
</table>

The maximum electric field of the device is 5.07x10^6 V/cm, and it is obtained for drain voltage of 625V. The minimum electric field of the device is 2.20x10^6 V/cm, and it is obtained for drain voltage of 100V. From Equation 4.6 as the drain voltage increases from 100V to 625V, the electric field of the device increases. This is due to the fact that a direct relation exists between drain voltage and electric field.

4.4 Surface Temperature of Device Using COMSOL Multiphysics

The one-directional 3C-SiC MESFET is simulated in COMSOL Multiphysics and surface temperature of the device is investigated. The procedure begins by computing power dissipation in Silvaco Atlas. This power dissipation is imported to COMSOL as the heat source of the thermal model. The three-dimensional finite element model generated by COMSOL is used to obtain temperature distribution in the thermal model according to the defined heat source [26]. From Figure 4.13, it shows the surface temperature of the device for fixed gate voltage of 0V and different drain voltages. Figure 4.13(a) shows the maximum surface temperature of the device for drain voltage of 625V and gate voltage of 0V is 350K obtained at drain end.
Figure 4.13 Surface temperature of device at gate voltage of 0 V and (a) drain voltage of 625V, (b) drain voltage of 500V.
Figure 4.13 continued. Surface temperature of device at gate voltage of 0 V and (C) drain voltage of 400V, (d) drain voltage of 300 V.
Figure 4.13 continued. Surface temperature of device at gate voltage of 0 V and (e) drain voltage of 200 V, and (f) drain voltage of 100 V.
This is due to power (heat source) concentrated at drain end [26-27]. Power is the product of drain current and drain voltage [26-27]. From Figure 4.1(a) the drain current of the device is 0.6mA, and drain voltage is 625V. The amount of power at drain end is 0.375 watts. The temperature of the source is fixed to 293K [26-27].

Figure 4.13(b) shows the maximum surface temperature of the device for drain voltage of 500V and gate voltage of 0V is 335K obtained at drain end. This is due to power (heat source) concentrated at the drain end [26-27]. Power is the product of drain current and drain voltage [26-27]. From Figure 4.1(a) the drain current of the device is 0.6mA, and drain voltage is 500V. The amount of power at drain end is 0.300 watts. The temperature of the source is fixed to 293K [26-27].

Figure 4.13(c) shows the maximum surface temperature of the device for drain voltage of 400V and gate voltage of 0V is 325K obtained at drain end. This is due to power (heat source) concentrated at the drain end [26-27]. Power is the product of drain current and drain voltage [26-27]. From Figure 4.1(a) the drain current of the device is 0.6mA, and drain voltage is 400V. The amount of power at drain end is 0.24 watts. The temperature of the source is fixed to 293K [26-27].

Figure 4.13(d) shows the maximum surface temperature of the device for drain voltage of 300V and gate voltage of 0V is 320K obtained at the drain end. This is due to power (heat source) concentrated at the drain end [26-27]. Power is the product of drain current and drain voltage [26-27]. From Figure 4.1(a) the drain current of the device is 0.6mA, and drain voltage is 300V. The amount of power at drain end is 0.180 watts. The temperature of the source is fixed to 293K [26-27].
Figure 4.13(e) shows the maximum surface temperature of the device for drain voltage of 200V and gate voltage of 0V is 310K obtained at drain end. This is due to power (heat source) concentrated at the drain end [26-27]. Power is the product of drain current and drain voltage [26-27]. From Figure 4.1(a) the drain current of the device is 0.6mA, and drain voltage is 200V. The amount of power at drain end is 0.120 watts. The temperature of the source is fixed to 293K [26-27].

Figure 4.13(f) shows the maximum surface temperature of the device for drain voltage of 100V and gate voltage of 0V is 302K obtained at drain end. This is due to power (heat source) concentrated at the drain end [26-27]. Power is the product of drain current and drain voltage [26-27]. From Figure 4.1(a) the drain current of the device is 0.6mA, and drain voltage is 100V. The amount of power at drain end is 0.06 watts. The temperature of the source is fixed to 293K [26-27]. From Figure 4.13, surface temperature of the device increases due to increases in power (heat source) at drain end [26-27].

4.4.1 Surface temperature of the device for fixed drain voltage and different gate voltages

The one-directional 3C-SiC MESFET is simulated for fixed drain voltage and different gate voltages. Figure 4.14 shows the surface temperature of the device for fixed drain voltage of 625V and various gate voltages. In Figure 4.14(a), the maximum surface temperature of the device for drain voltage of 625V, gate voltage of -1V is 315K at drain end, and this is due to power (heat source) concentrated at drain end [26-27]. Power is the product of current and voltage [26-27]. From Figure 4.1, the drain current for a gate voltage of -1V is 0.3mA, drain voltage is 625V, and the power is 0.187 watts. The source end is fixed at 293K [26-27].
From Figure 4.14(b), the maximum surface temperature of the device for drain voltage of 625V, gate voltage of -2V is 308K at drain end, and this is due to power (heat source) concentrated at drain end [26-27]. Power is the product of current and voltage [26-27]. From Figure 4.1, the drain current for a gate voltage of -2V is 0.25mA, and drain voltage is 625V, and the power is 0.156 watts. The source end is fixed at 293K [26-27].

From Figure 4.14(c), the maximum surface temperature of the device for drain voltage of 625V, gate voltage of -3V is 301K at drain end, and this is due to power (heat source) concentrated at drain end [26-27]. Power is the product of current and voltage [26-27]. For Figure 4.1, the drain current for gate voltage of -3V is 0.15mA, and drain voltage is 625V, and the power is 0.093 watts. The source end is fixed at 293K [26-27].

For Figure 4.14(d), the maximum surface temperature of the device for drain voltage of 625V, gate voltage of -4V is 297K at drain end, and this is due to power (heat source) concentrated at drain end [26-27]. Power is the product of current and voltage [26-27]. From Figure 4.1, the drain current for gate voltage of -4V is 0.1mA, and drain voltage is 625V, and the power is 0.062 watts. The source end is fixed at 293K [26-27]. For Figure 4.14, as the power decreases from 0.192 watts to 0.064 watts, the surface temperature decreases from 315K to 297K [26-27].
Figure 4.14. Surface temperature of device for drain voltage of 625 V and gate voltage of (a) -1V, (b) -2V.
Figure 4.14 continued. Surface temperature of device for drain voltage of 640 V and gate voltage of (c) -3 V, and (d) -4 V.
Table 4.9 shows the dependence of the drain voltage on surface temperature of the device. The one-directional 3C-SiC MESFET surface temperature is simulated for different drain voltages and results are plotted in Figure 4.15. For Figure 4.15, the surface temperature of the device dependence is on applied drain voltage [28]. As the drain voltage increases from 100V to 625V, with gate voltage of 0V the surface temperature increases from 302K to 352K. From Figure 4.1(a) the drain current is 0.6mA. In the device heating model, the device uses power derived from forced current multiplied by the potential [26]. Each charge carrier in the current traverses the potential work that is done on the charge, and this energy in IV model is all assumed to go into heating the device [26].

Table 4.9 Dependence of temperature on drain voltage of the device

<table>
<thead>
<tr>
<th>Temperature (k)</th>
<th>Drain voltage (volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>352</td>
<td>625</td>
</tr>
<tr>
<td>339</td>
<td>500</td>
</tr>
<tr>
<td>330</td>
<td>400</td>
</tr>
<tr>
<td>321</td>
<td>300</td>
</tr>
<tr>
<td>312</td>
<td>200</td>
</tr>
<tr>
<td>302</td>
<td>100</td>
</tr>
</tbody>
</table>

Figure 4.15 Drain voltage versus Temperature of the device [28].
CHAPTER 5

CONCLUSION AND FUTURE WORK

The vertical MESFET has many advantages over conventional SiC and Si devices. The device has a new structure that provides many potential advantages. The first is that the SiC layers can be easily grown on a large area of Si substrates. This results in low-cost fabrication process. The second is that the area occupied by the device is less than 50% the area occupied by conventional Si devices. This is because the source, gate, and drain are on top of each other. The third is that the device can be easily cooled, as the active region of the channel becomes accessible to the cooling medium.

The device breakdown voltage was found to be 625V. Although this value is not as high as silicon power devices, which can achieve breakdown voltages of more than 1000V, an optimized device can achieve much higher breakdown voltages. This can be achieved by optimizing the device structure to eliminate local breakdown regions. Our device has not yet been optimized for power applications, since the scope of the thesis was to validate the vertical structure before optimizing the structure for breakdown voltages.

Future work based on this thesis includes optimizing the device to increase the breakdown voltage, conducting thermal analysis by applying cooling techniques to test the endurance of the device at extreme working condition fabricating and testing the device, and comparing with simulation results for further optimization of the device geometry.
REFERENCES


## APPENDIX

### NUMERICAL CALCULATIONS USING MATHCAD

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Channel thickness</td>
</tr>
<tr>
<td>L</td>
<td>Gate length</td>
</tr>
<tr>
<td>Z</td>
<td>Gate width</td>
</tr>
<tr>
<td>Q</td>
<td>Charge of electron</td>
</tr>
<tr>
<td>E</td>
<td>Permittivity of 3C-SiC</td>
</tr>
<tr>
<td>$E_g$</td>
<td>Energy band-gap of 3C-SiC</td>
</tr>
<tr>
<td>W</td>
<td>Depletion width</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Mobility of electrons</td>
</tr>
<tr>
<td>$V_{bi}$</td>
<td>Built-in potential</td>
</tr>
<tr>
<td>$N_d$</td>
<td>Doping concentration</td>
</tr>
<tr>
<td>$V_{po}$</td>
<td>Pinchoff voltage</td>
</tr>
<tr>
<td>$V_g$</td>
<td>Gate voltage</td>
</tr>
<tr>
<td>$V_d$</td>
<td>Drain voltage</td>
</tr>
<tr>
<td>$V_t$</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>$E_p$</td>
<td>Critical electric field</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current</td>
</tr>
<tr>
<td>$I_{D\text{ sat}}$</td>
<td>Drain saturation current</td>
</tr>
</tbody>
</table>

\[
\varepsilon := 10\varepsilon_0
\]

\[
\varepsilon = 8.854 \times 10^{-13} \text{ F. cm}^{-1}
\]

The energy band-gap of 3C-SiC is 2.20V

\[
E_g := 2.20V
\]

\[
V_{bi} := \left(\frac{2}{3}\right) \cdot E_g
\]

\[
V_{bi} = 1.467 \text{ V}
\]

\[
N_d := 1 \cdot 10^{17} \text{ cm}^{-3}
\]
\[ q := 1.610^{-19} \text{C} \]
\[ a := 0.2310^{-6} \text{m} \]

\[ W := \sqrt{\frac{2\varepsilon V_{bi}}{qN_{d}}} \]

\[ W = 1.274 \times 10^{-7} \text{m} \]

\[ V_{po} := \frac{qN_{d}a^{2}}{2\varepsilon} \]

\[ V_{po} = 5.647 \text{V} \]

\[ V_{t} := V_{bi} - V_{po} \]

\[ V_{t} = -4.18 \text{V} \]

For gate voltage \((V_{g} = 0 \text{V})\)

\[ V_{Dsat} := V_{po} + V_{g} - V_{bi} \]

\[ V_{Dsat} = 4.18 \text{V} \]

\[ L := 1.10^{-6} \text{m} \]

\[ Z := 2.10^{-6} \text{m} \]

\[ \mu_{n} := 0.09 \text{m}^{2} \text{s}^{-1} \text{V}^{-1} \]

\[ I_{p} := \frac{q\mu_{n}N_{d}Z \varepsilon V_{po}}{L} \]
From the MATHCAD calculations the threshold voltage of the device is -4.18V. The drain current is calculated for gate voltage of 0V, drain voltage of 4V is 0.6mA, and drain saturation current is 0.658mA. The critical breakdown electric field of the device is 2.259x10^7 V/cm. The numerical simulator Silvaco Atlas shows that the device has threshold
voltage -4.75V, the drain current is 0.6mA, and the critical electric field is 3.9x10^6 V/cm. To calculate the built-in potential, the MATHCAD takes \( \frac{2}{3} E_g \) as formula; due to that, there is some difference in threshold voltage of theoretical and simulation methods.